CLAIMS

1. A circuit comprising:

a memory element defining a semaphore allocatable to a resource; and

a controller configured to (i) present a granted status in response to a processor reading a first address while said semaphore has a free status, (ii) set said semaphore to a busy status in response to presenting said granted status, and (iii) present said busy status in response to said processor reading said first address while said semaphore has said busy status.

2. The circuit according to claim 1, wherein said controller is further configured to set said semaphore to said free status in response to said processor writing to said first address.

3. The circuit according to claim 1, wherein said controller is further configured to present said status of said semaphore in response to said processor reading a second address.

4. The circuit according to claim 3, wherein said controller is further configured to maintain said status of said

semaphore in response to said processor writing to said second address.

5. The circuit according to claim 1, further comprising:

a second memory element defining a second semaphore allocatable to said semaphore; and

a second controller configured to (i) present said granted status in response to said processor reading a third address while said second semaphore has said free status, (ii) set said second semaphore to said busy status in response to presenting said granted status, (iii) present said busy status in response to said processor reading said third address while said second semaphore has said busy status, and (iv) set said second semaphore to said free status in response to said processor writing to said third address.

6. The circuit according to claim 5, wherein said controller is further configured to:

slave said semaphore to said second semaphore;

present said busy status in response to said processor reading said first address while said second semaphore has said busy status; and

maintain said busy status for said semaphore in response to said processor writing to said first address while said second semaphore has said busy status.

7. The circuit according to claim 6, wherein said controller is further configured to set said semaphore to said free status in response to said processor writing to said third address.

8. The circuit according to claim 6, wherein said controller is further configured to maintain said busy status for said semaphore in response to said processor writing to said third address.

9. A method of allocating a resource to a processor comprising the steps of:

(A) defining a semaphore allocatable to said resource;

(B) presenting a granted status in response to said processor reading a first address while said semaphore has a free status;

(C) setting said semaphore to a busy status in response to presenting said granted status; and

(D) presenting said busy status in response to said processor reading said first address while said semaphore has said busy status.

10. The method according to claim 9, further comprising the step of setting said semaphore to said free status in response to said processor writing to said first address.

11. The method according to claim 9, further comprising the step of presenting said status of said semaphore in response to said processor reading a second address.

12. The method according to claim 11, further comprising the step of maintaining said status of said semaphore in response to said processor writing to said second address.

13. The method according to claim 9, further comprising the steps of:

defining a second semaphore allocatable to said semaphore;

second presenting said granted status in response to said processor reading a third address while said second semaphore has said free status;

setting said second semaphore to said busy status in response to said second presenting of said granted status;

presenting said busy status in response to said processor reading said third address while said second semaphore has said busy status; and

setting said second semaphore to said free status in response to writing to said third address.

14. The method according to claim 13, further comprising the steps of:

slaving said semaphore to said second semaphore;

presenting said busy status in response to said processor reading said first address while said second semaphore has said busy status;

maintaining said busy status for said semaphore in response to said processor writing to said first address while said second semaphore has said busy status.

15. The method according to claim 14, further comprising the step of setting said semaphore to said free status in response to said processor writing to said third address.

16. The method according to claim 14, further comprising the step of maintaining said busy status for said semaphore in response to said processor writing to said third address.

17. A circuit comprising:

means for defining a semaphore allocatable to a resource;

means for presenting a granted status in response to a processor reading a first address while said semaphore has a free status;

means for setting said semaphore to a busy status in response to presenting said granted status; and

means for presenting said busy status in response to said processor reading said first address while said semaphore has said busy status.